PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| Appl. No. | : | 10/655,854 |
| Applicant | : | Rafael Reif et al. |
| Filed | : | September 5, 2003 |
| T.C./A.U. | : | 2826 |
| Examiner | : | Leonardo Andujar |
| Docket No. | : | MIT-136AUS |
| Customer No. | : | 022494 |

Confirmation No.: 7254

RESPONSE TO NOTICE OF ABANDONMENT
(OR IN THE ALTERNATIVE PETITION TO REVIVE UNDER 37 C.F.R. §1.137(b)

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Abandonment dated June 26, 2008, enclosed please find the following documents:

1. Copy of a submission made on April 11, 2008 by facsimile which includes:
   a. a receipt from Applicant's facsimile machine showing that 24 pages were successfully transmitted to the U.S. Patent and Trademark Office (PTO) on April 11, 2008
   b. a facsimile cover sheet indentifying a 24 page facsimile submission;
   c. a Request for Continued Examination (RCE);
   d. a Supplemental Amendment under 37 C.F.R. §1.116; and
   e. a Request for an Extension of Time;

2. a Copy of Auto-Reply Facsimile Transmission evidencing receipt of the above documents by the U.S. PTO on April 11, 2008 (kindly note that the Auto-Reply document generated by the US PTO confirms that 24 pages were received in the U.S. PTO on April 11, 2008 and that this matches the number of pages included in Applicant's facsimile submission); and

3. Copy of Notice of Abandonment dated June 26, 2008.

In view of the above RCE and amendment submitted by facsimile on April 11, 2008 as well as the Auto-Reply return receipt provided by the US PTO evidencing receipt of the submission at the US PTO on April 11, 2008, Applicant submits that the Notice of Abandonment was issued in error and Applicant respectfully requests that the Notice of Abandonment be withdrawn and that prosecution be re-opened in this case.

In the alternative, Applicant respectfully requests that the US PTO treat this submission as a Petition to Revive under 37 C.F.R. §1.137(b) (Unintentional). Applicant requests that the Petition fee be waived, but Applicant authorizes the US PTO to deduct any underpayment or credit any overpayment of the Petition Fee from/to Deposit Account No. 50-0845. Applicant states that if any delay is found in submitting the required reply from the due date for the reply until the filing of this petition, that the entire delay was unintentional.

In the event that Applicant is charged the Petition Fee required by 37 C.F.R. §1.137(b), Applicant requests that this submission also be considered as a Petition for Refund of the Petition Fee. It appears clear from the record that a timely submission was made and received by the US PTO and that the Notice of Abandonment was issued in error.

Please do not hesitate to contact the below signing attorney if there are any questions regarding this submission or this application.

Respectfully submitted,

Dated: 2 Jul 2008

DALY, CROWLEY, MOFFORD & DURKEE, LLP

By: /csd/

Christopher S. Daly
Reg. No. 37,303
Attorney for Applicant(s)
354A Turnpike Street - Suite 301A
Canton, MA 02021-2714
Tel.: (781) 401-9988, Ext. 111
Fax: (781) 401-9966
*csd@dc-m.com*

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TRANSMISSION VERIFICATION REPORT

TIME : 05/17/2000 16:22
NAME : DCMD
FAX : 7814019966
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| DATE,TIME | 05/17 16:15 |
| FAX NO./NAME | 915712738300 |
| DURATION | 00:06:59 |
| PAGE(S) | 24 |
| RESULT | OK |
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# DALY, CROWLEY, MOFFORD & DURKEE, LLP

**Telephone: 781-401-9988**
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FACSIMILE TRANSMITTAL SHEET

Including this transmittal sheet, document consists of 24 pages.

Date: April 11, 2008

| | | | |
|---|---|---|---|
| **To:** | **Commissioner for Patents** | From: | Christopher S. Daly, Esq. |
| Examiner: | Leonardo Andujar | | |
| Group Art: | 2826 | | |
| Company: | U.S. PTO | | |
| **Facsimile Number:** | **571-273-8300** | | |
| Telephone Number: | | | |

**MESSAGE**

RE: U.S. Patent Application of Rafael Reif et al.
Entitled: Multi-Layer Integrated Semiconductor Structure
Filed on: September 5, 2003
**U.S. Appl. No.: 10/655,854**
Our Ref. No.: MIT-136AUS

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# DALY, CROWLEY, MOFFORD & DURKEE, LLP

**Telephone: 781-401-9988**
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FACSIMILE TRANSMITTAL SHEET

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| Examiner: | Leonardo Andujar | | |
| Group Art: | 2826 | | |
| Company: | U.S. PTO | | |
| **Facsimile Number:** | **571-273-8300** | | |
| Telephone Number: | | | |

**MESSAGE**

RE: U.S. Patent Application of Rafael Reif et al.
Entitled: Multi-Layer Integrated Semiconductor Structure
Filed on: September 5, 2003
**U.S. Appl. No.: 10/655,854**
Our Ref. No.: MIT-136AUS

**PLEASE CONFIRM RECEIPT OF THIS FACSIMILE TRANSMISSION.**

**THANK YOU.**



IF THERE IS A PROBLEM WITH THIS TRANSMISSION, OR IF YOU DID NOT RECEIVE ALL PAGES, PLEASE CALL 781-401-9988 AS SOON AS POSSIBLE

PTO/SB/21 (01-08)
Approved for use through 01/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

| | |
|---|---|
| Total Number of Pages in This Submission | 23 |

| | |
|---|---|
| Application Number | 10/655,854 |
| Filing Date | September 5, 2003 |
| First Named Inventor | Rafael Reif |
| Art Unit | 7254 |
| Examiner Name | Leonardo Andujar |
| Attorney Docket Number | MIT-136AUS |

## ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☑ Amendment/Reply
  - ☑ After Final
  - ☐ Affidavits/declaration(s)
- ☑ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

PTO/SB30 Request for Continued Examination

**Remarks**

In the event a petition for extension of time is required by this paper and not otherwise provided, such petition is hereby made and authorization is provided herewith to charge deposit account No. 50-0845 for the cost of such extension.

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | | | |
|---|---|---|---|
| Firm Name | Daly, Crowley, Mofford & Durkee, LLP | USPTO Customer No | 022494 |
| Signature | /csd/ | | |
| Printed name | Christopher S. Daly | | |
| Date | 11 Apr 2008 | Reg. No. | 37,303 |

## CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

| | | | |
|---|---|---|---|
| Signature | Mary H. White | | |
| Typed or printed name | Mary H. White | Date | 11 Apr 2008 |

PTO/SB/30 (10-07)
Approved for use through 10/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


# Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

| | |
|---|---|
| Application Number | 10/655,854 |
| Filing Date | September 5, 2003 |
| First Named Inventor | Rafael Reif |
| Art Unit | 2826 |
| Examiner Name | Leonardo Andujar |
| Attorney Docket Number | MIT-136AUS |

**This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.**
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____ _____

      Ii. ☐ Other _____

   b. ☑ Enclosed

      I. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to

   a. ☑ Deposit Account No. 500845. I have enclosed a duplicate copy of this sheet.

      i. ☑ RCE fee required under 37 CFR 1.17(e)

      ii. ☑ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

***SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED***

| | | | |
|---|---|---|---|
| Signature | /csd/ | Date | 11 Apr 2008 |
| Name (Print/Type) | Christopher S. Daly | Registration No. | 37,303 |

***CERTIFICATE OF MAILING OR TRANSMISSION***

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

| | | | |
|---|---|---|---|
| Signature | Mary H. White | | |
| Name (Print/Type) | Mary H. White | Date | 11 Apr 2008 |

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| Appl. No. | : | 10/655,854 | Confirmation No.: 7254 |
| Applicant | : | Rafael Reif, et al. | |
| Filed | : | September 5, 2003 | |
| T.C./A.U. | : | 2826 | |
| Examiner | : | Leonardo Andujar | |
| | | | |
| Docket No. | : | MIT-136AUS | |
| Customer No | : | 22494 | |

**SUPPLEMENTAL AMENDMENT UNDER 37 C.F.R. §1.116**

Mail Stop After Final
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Final Office Action dated May 10, 2007 and further to the Notice of Appeal dated October 11, 2007 and the Advisory Action dated November 14, 2007, please amend the above-identified patent application as follows under the provisions of 37 C.F.R §1.116.

**Amendments to the Specification** begin on page 2 of this paper.

**A listing of the Claims** are reflected in the listing of claims, which begins on page 4 of this paper.

**Remarks** begin on page 14 of this paper.

**An Appendix** including Exhibits A and B is attached following page 19 of this paper.

Amendments to the Specification:

Please replace the paragraph beginning at page 19, line 18 with the following amended paragraph.

Referring to Fig. 6, an embodiment of a die-to-wafer structure 70 is provided, which includes a first die 72 disposed over and coupled to a second die 76, via a conductive bond film 74a. Optionally, the bond film 74b, e.g., adhesive material, may also be provided to further strengthen the bond formed between the first die 72 and the second die 76, which is provided as part of a larger integrated circuit or wafer 78. The bond films 74a and 74b or segments may be provided as any of the types described above in conjunction with Figs. 1-4 (e.g., conductive interface portion 38 and interface portion 41, respectively) and serves to bond the first die 72 to the second die 76, as described above. Thus, to provide the die-to-wafer structure 70, the bond films 74a, 74b can be first applied to a wafer (not shown) of which the first die 72 is a part. While the first die 72 is part of the wafer, the bond film can be patterned or otherwise disposed on the die 72 using a variety of different techniques, including those techniques described in copending U.S. Patent Application Serial No. 10/655,670 (now U.S. Patent No. 7064055)[_____], filed on September 5, 2003, which is entitled METHOD OF FORMING A MULTI-LAYER SEMICONDUCTOR STRUCTURE HAVING A SEAMLESS BONDING INTERFACE, which is commonly assigned to the Assignee of the present application and which is hereby incorporated by reference in its entirety. Once the bond films 74a, 74b are disposed on the wafer including the first die 72, the first die 72 is cut or otherwise separated from the wafer.

Please replace the paragraph beginning at page 20, line 16 with the following amended paragraph.

Once the first die 72 and the second die 76 are properly aligned, at least the first die 72 is exposed to a method for bonding the first and second dies 72, 76, via the bond films 74a, 74b,

which is similar to that described in Fig. 1 of commonly assigned U.S. Patent Application Serial No. 10/655,670, (now U.S. Patent No. 7064055) [ _____,] as described above. The particular temperatures and pressures used for bonding the first and second dies 72, 76 will depend upon a variety of factors, including but not limited to, the specific material from which the bond film 74 is provided, as well as the size, shape and material from which the first die 72 is provided, as well as the size, shape and material from which the second die 76 is provided.

Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

1. (Previously Presented) A multi-layer integrated semiconductor structure, comprising:

(a) a first device layer having first and second opposing surfaces, said first device layer including:

a first substrate having a first surface corresponding to the first surface of the first device layer and having a second opposing surface, the first substrate having provided therein a first plurality of doped regions which form at least part of one or more semiconductor elements;

a dielectric material having first and second opposing surfaces with the first dielectric material surface disposed over the second surface of the first substrate and wherein the second surface of the dielectric material corresponds to the second surface of the first device layer; and

a first conductive via provided in the dielectric material, the first conductive via having a first end electrically coupled to at least one of the first plurality of doped regions and a second end exposed through the second one of the first and second surfaces of the dielectric material;

(b) a conductive interface having a first surface and a second opposing surface with the first surface of the conductive interface disposed over at least a portion of the second surface of the dielectric material such that at least a portion of the conductive interface is coupled to at least a portion of the first end of the first conductive via in the first device layer;

(c) a second device layer having first and second opposing surfaces, with the first surface of said second device layer disposed over the second surface of the conductive interface, the second device layer including:

a second substrate having first and second opposing surfaces and having provided therein a second plurality of doped regions which form at least part of one or more semiconductor elements;

an insulating material having a first surface disposed against the second opposing surface of the conductive interface and a second opposing surface of the insulating material disposed against a first one of the first and second opposing surfaces of the second substrate and wherein the second device layer is secured to the first device layer via the conductive interface; and

a second conductive via provided in the second device layer, said second conductive via having a first end directly coupled to the conductive interface and having a second end coupled to at least one of the second plurality of doped regions such that an electrical communication path between the first device layer and the second device layer is provided by the first conductive via, the conductive interface and the second conductive via.

2. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1 further comprising a first conductive interconnect element disposed in the dielectric material of the first device layer with a first end of the first conductive interconnect element coupled to the first conductive via and a second end of the first conductive interconnect element coupled to at least one of the first plurality of doped semiconductor elements.

3. (Cancelled)

4. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1 further comprising a second conductive interconnect having a first portion disposed over at least a portion of one of the second plurality of doped regions and having a second portion coupled to the second end of the second conductive via.

5. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, further comprising a second conductive interconnect disposed in the second device layer and coupled to the second conductive via provided in the second device layer.

6. (Previously Presented) The multi-layer integrated semiconductor structure of claim 5, wherein the second conductive interconnect is coupled to at least one of the one or more semiconductor elements of the second device layer.

7. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, wherein the second conductive via includes a first end coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

8. (Previously Presented) The multi-layer integrated semiconductor structure of claim 7, wherein the second device layer comprises a second conductive interconnect having a first portion coupled to the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive via to the at least one element of the second plurality of semiconductor elements..

9. (Cancelled)

10. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1 further comprising a third conductive via provided in the first device layer, wherein the third conductive via is coupled between a portion of the first conductive interconnect and the at least one of the first plurality of doped regions.

11. (Previously Presented) The multi-layer integrated semiconductor structure of claim 10 further comprising a second conductive interface disposed over a first surface of the second device layer and wherein the second conductive via forms at least a part of an electrical communication path between the second conductive interconnect and at least a portion of the second interface.

12. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, wherein the first conductive via forms at least a portion of a signal path between the conductive interface and at least one of the first and second plurality of semiconductor elements.

13. (Previously Presented) The multi-layer integrated semiconductor structure of claim 12, wherein the second end of the first conductive via is coupled to the at least one element of the first plurality of semiconductor elements.

14. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, wherein the first conductive interface comprises copper.

15. (Previously Presented) The multi-layer integrated semiconductor structure of claim 14 wherein the conductive interface is provided as a first conductive interface region and the multi-layer integrated semiconductor structure further comprises a second conductive interface region disposed between the first and second device layers with the second conductive interface region being physically separated from the first conductive interface region.

16. (Previously Presented) The multi-layer integrated semiconductor structure of claim 15, wherein the second interface region includes an adhesive material such that the second interface region secures the first device layer to the second device layer.

17. (Previously Presented) A multi-layer integrated semiconductor structure, comprising:

(a) at least a first device layer having first and second opposing surfaces, said first device layer including:

a first substrate having a first surface corresponding to the first surface of the first device layer and having a second opposing surface, the first substrate having provided therein at least a first doped semiconductor region which forms at least part of one or more semiconductor elements; and

a first dielectric material having first and second opposing surfaces with the first dielectric material surface disposed about the first doped semiconductor region and wherein the

second surface of the first dielectric material corresponds to the second surface of the first device layer, said dielectric material having at least a first via-hole with a first conductive material disposed therein to provide a first conductive via having first and second opposing ends with a first one of the first and second ends of the first conductive via electrically coupled to a at least a portion of at least one of the one or more semiconductor elements and a second one of the first and second ends of the first conductive via exposed through the second surface of the first dielectric material; and

(b) at least a second device layer having first and second opposing surfaces, with the first surface of said second device layer including:

a second substrate having first and second opposing surfaces and having provided therein at least a second doped semiconductor region which forms at least part of one or more semiconductor elements; and

a second dielectric material having first and second opposing surfaces with the first dielectric material surface disposed about the second doped semiconductor region and the second surface of the second dielectric material corresponding to the second surface of the second device layer and wherein said second substrate includes a second via-hole having a second conductive material disposed therein to provide a second conductive via having first and second ends with a first one of the first and second ends of the second conductive via electrically coupled to at least a portion of at least one of the one or more semiconductor elements of the second substrate and a second one of the first and second ends of the second conductive via is exposed through the second surface of the second dielectric material; and

(c) a first conductive interface having a first surface and a second opposing surface with the first surface of the conductive interface disposed between at least a portion of a first one of the first and second opposing surfaces of the first device layer and at least a portion of a first one of the first and second opposing surfaces of the second device layers such that at least a portion of the first conductive interface secures together the first and second device layers and also electrically couples the first device layer to the second device layer wherein the conductive interface and the first and second conductive vias form at least a portion of an electrical communication path between the first device layer and the second device layer.

18. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17 further comprising a first conductive interconnect element disposed in the first device layer with a first portion of the first conductive via electrically coupled to at least a portion of the first conductive interconnect element and a second portion of the first conductive interconnect element coupled to the first doped semiconductor region.

19. (Previously Presented) The multi-layer integrated semiconductor structure of claim 18, wherein the first conductive via couples the first conductive interconnect element to the first conductive interface.

20. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and is coupled to the second doped semiconductor region.

21. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17 further comprising a third conductive via coupled to the second doped semiconductor region.

22. (Previously Presented) The multi-layer integrated semiconductor structure of claim 21 further comprising a second conductive interface disposed on the second one of the first and second opposing surfaces of the second device layer and wherein the third conductive via is provided having a first end coupled to the second doped semiconductor region and a second end coupled to the second conductive interface.

23. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and wherein the second device layer further comprises a first conductive interconnect.

24. (Previously Presented) The multi-layer integrated semiconductor structure of claim 23, wherein the second conductive via is provided having a first end coupled to the first conductive

interconnect and a second end coupled to the first conductive interface.

25. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive via is coupled to at least the first doped semiconductor region.

26. (Previously Presented) The multi-layer integrated semiconductor structure of claim 25, wherein the first conductive via is provided having a first end coupled to at least the first doped semiconductor region and a second end coupled to the first conductive interface.

27. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first interface corresponds to a first conductor interface region and the multi-layer integrated semiconductor structure further comprises a second interface region disposed between the first one of the first and second device layers with the second interface region provided from a non-conductive material.

28. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive interface region is provided from a conductive bonding material.

29. (Previously Presented) The multi-layer integrated semiconductor structure of claim 18, further comprising a second conductive interconnect element disposed in the second device layer with a portion of the second conductive interconnect element coupled to the second conductive via and wherein the first conductive via, the first conductive interface and the second conductive via provide a direct vertical electrical connection between the first conductive interconnect element and the second conductive interconnect element.

30. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.

31. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.

32. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element.

33. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element.

34. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

35. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

36. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.

37. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area which is substantially equivalent to the first predetermined surface area.

38. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer further comprises:

a first conductive interconnect element having a first portion coupled to the first doped semiconductor region, and a second portion coupled to a first end of the first conductive via.

39. (Previously Presented) The multi-layer integrated semiconductor structure of claim 38, wherein the second device further comprises a second conductive interconnect element having a first portion coupled to the second doped semiconductor region and a second portion coupled to a first end of the second conductive via with the second end of the first conductive via and the second end of the second conductive via each coupled to the first interface.

40. (Previously Presented) A multi-layer semiconductor structure, comprising:

a first semiconductor wafer having first and second opposing surfaces, said first semiconductor wafer including a first plurality of semiconductor structures each of which includes a first plurality of semiconductor elements, said first semiconductor wafer also comprising a first plurality of conductive vias, at least some of said first plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least some of said first plurality of semiconductor elements and a second end is exposed through one of the first and second surfaces of the first semiconductor wafer;

a second semiconductor wafer having first and second opposing surfaces, said second semiconductor wafer including a second plurality of semiconductor structures each of which includes a second plurality of semiconductor elements, said second semiconductor wafer also comprising a second plurality of conductive vias, at least some of said second plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least some of said second plurality of semiconductor elements and a second end is exposed through one of the first and second surfaces of the second semiconductor wafer; and

at least a first conductive bonding interface segment disposed between a first one of the first and second opposing surfaces of the first semiconductor wafer and a first one of the first and second opposing surfaces of the second semiconductor wafer, said first conductive bonding interface segment disposed over at least a first one of the plurality of semiconductor structures of the first semiconductor wafer and being in an electrical communication relationship through the first plurality of conductive vias electrically coupled to the first plurality of semiconductor

elements with at least a first one of the first plurality of the semiconductor elements of the first semiconductor structure and at least a first one of the plurality of semiconductor elements of the second semiconductor structure of the second semiconductor wafer where the first conductive bonding interface segment and at least some of the first and second plurality of conductive vias form electrical signal paths between at least some of the first semiconductor elements of the first semiconductor structure and at least some of the second semiconductor elements of the second semiconductor structure.

41. Cancelled.

Please add the following new claim:

42. (New) A multi-layer semiconductor structure, comprising:

a first semiconductor wafer having first and second opposing surfaces, said first semiconductor wafer including a first plurality of semiconductor structures each of which includes a first plurality of semiconductor elements, said first semiconductor wafer also comprising a first plurality of conductive vias, at least some of said first plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least some of said first plurality of semiconductor elements and a second end is exposed through one of the first and second surfaces of the first semiconductor wafer;

a second semiconductor wafer having first and second opposing surfaces, said second semiconductor wafer including a second plurality of semiconductor structures each of which includes a second plurality of semiconductor elements, said second semiconductor wafer also comprising a second plurality of conductive vias, at least some of said second plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least some of said second plurality of semiconductor elements and a second end is exposed through one of the first and second surfaces of the second semiconductor wafer; and

a conductive bonding interface segment disposed between a first one of the first and second opposing surfaces of the first semiconductor wafer and a first one of the first and second opposing surfaces of the second semiconductor wafer said conductive bonding interface segment bonding together said first and second semiconductor wafers and forming at least part of an

electrical communication path between at least one of the first plurality of semiconductor structures on said first semiconductor wafer and at least one of the first plurality of semiconductor structures on said second semiconductor wafer.

REMARKS

Applicants respectfully request the Examiner to reconsider and again examine the claims in accordance with the provisions of 37 C.F.R §1.116.

This Supplemental Amendment under 37 C.F.R. §1.116 is being filed with a Request for Continued Examination (RCE) for the purpose of adding independent claim 42 to further define Applicants' patentable subject matter.

Claims 1, 2, 4-8 and 10-40 are pending in the application. No Claims are amended by this amendment. Claims 1, 2 and 10-40 are rejected. Claims 3, 9 and 41 have been cancelled by previous amendments. Claim 42 is newly added by this amendment. No claims have been cancelled by this amendment. Claims 1, 17, and 40 and 42 are independent claims.

Applicants submit that claim 42 is patentable over the prior art of record in this case since the prior art neither describes nor suggests "... a ... conductive bonding interface segment bonding together said first and second semiconductor wafers **and** forming at least part of an electrical communication path between ... semiconductor structures on said first and second semiconductor wafer[s]..." as called for in claim 42.

The arguments presented in the Response filed on or about October 9, 2007 (in response to the Office Action dated May 10, 2007) are repeated below for the Examiner's convenience.

The Examiner again rejects claims 1, 2, 4-8, 10-13 and 17 - 40 under 35 U.S.C. §102(b) as being anticipated by Koyanagi (U.S. Pat. No. 6,525,415). To sustain a rejection under 35 U.S.C. §102(b), a single reference must disclose each and every element of the claimed invention. In this case, as will be explained further herein, the Koyanagi reference fails to describe or suggest a conductive interface which forms at least part of an electrical communication path and **secures** together first and second device layers as called for in each of

independent claims 1 and 17. In addition, as also further explained herein, Koyanagi likewise fails to describe or suggest claim 40's recitation of a first conductive **bonding** interface segment disposed between two wafers and which also provides electrical connections between at least some semiconductor elements of the first and second wafers.

In the Office Action, the Examiner equates the "microbumps" in the Koyanagi reference to the "conductive interface" recited in independent claims 1 and 17. Applicants have carefully reviewed and considered the Koyanagi reference, especially regarding the microbumps, and, as explained further below, Applicants again maintain that the primary function of the Koyanagi microbumps is to provide electrical connections, and Applicants further maintain that the Koyanagi microbumps cannot secure substrates together, as recited in claims 1, 17, and 40. Applicants will clarify further herein why this assertion is believed to be incorrect.

First, each of independent Claims 1 and 17 require that the conductive interface form at least part of an electrical communication path and secure together the first and second device layers. Similarly, independent claim 40 requires a first conductive bonding interface segment disposed between two wafers. Applicant's specification further explains at page 10, lines 9-16, that (a) the conductive interface at least couples (i.e., bonds together) the first and second device layers, (b) embodiments of the conductive interface can also electronically and/or photonically interconnect the device layers with each other; and (c) the conductive interface may provide "adhesive and/or bonding properties for securely coupling device layers 20 and 40" (emphasis provided).

Those of skill in the art readily understand what is meant in the claims and specification by the verbs "**secure**" and "**bond**." Specifically, as explained in the American Heritage College Dictionary (3rd Edition, 2000) (hereinafter "AH"), pages 158, and 1233 (copies of which are (hereinafter "RH") attached hereto as Exhibit A) and the Random House College Dictionary (Revised Edition, 1988) to "bond' means "*to join securely, as with glue or cement*"[AH]; "*to connect or bind; to join (two materials)*" [RH] and to "secure" means "*firmly fastened; to make tight or fasten*" [AH], "*to make firm or fast, as by attaching* [RH].

In sharp and direct contrast, Koyanagi states that the first and second substrates are instead tacked together, along the microbumps. This is done prior to being dipped into a fluid epoxy resin, which resin is processed such that it is injected wherever microbumps are absent, then the epoxy is injected around the microbumps then hardened to finally bond the two substrates together (see Koyanagi at col. 9, lines 28-55). It is thus specifically stated in Koyanagi that it is the epoxy (not the microbumps) which bonds the two substrates together. In some instances in Koyanagi, "in order to strengthen the tacking of the micro-bumps 42C and the microbumps 42D, pressure is uniformly applied between the substrates while monitoring the pressure with a load cell." (Koyanagi at col. 10, lines 44-46). However, as those of skill in the art recognize, tacking, even with pressure, is absolutely NOT the same thing as securing or bonding.

Moreover, Koyanagi NEVER teaches or suggests that this "tacking" is equivalent to or acting as any type of a **secure** fastening, nor does Koyanagi ever teach or suggest that the tacking of the microbumps is sufficient to secure the substrates together. To the contrary, as mentioned above, Koyanagi describes the epoxy as bonding together the two substrates. Koyanagi never provides any unique or special definitions of "tacking," but those of skill in the art readily understand what Koyanagi is referring to by "tacking." Consider the AH and RH definitions of "tack" as shown in the attached Exhibits A and B and listed in part below (at pages 1380 and 137, respectively), and compare them to the aforementioned definitions of "secure" and "bonding" as used in independent claims 1, 17, and 40:

Tack: To fasten or attach with or as if with a tack; to put together loosely or arbitrarily; [AH]; To secure by some slight or temporary fastening; to join together; unite; combine [RH]

Secure: To make tight or fasten; not likely to give way, stable; firmly fastened [AH]
To make firm or fast, as by attaching; dependable; firm; not liable to fail, yield, become displaced, etc., as a support or a fastening [RH].

Bond: To join securely, as with glue or cement [AH];

To connect or bind; to join (two materials); to hold together or cohere, as bricks in a wall or particles in a mass. [RH]

As the above definitions show, attachment by tacking is by definition is nearly the opposite of attachment by securing or attachment by bonding. Koyanagi also recognizes these limitations of tacking. That is why Koyanagi refers specifically to bonding the substrates together with epoxy adhesive (see, e.g., Koyanagi at col. 8, lines 5-21; col. 9, lines 28-55; col. 10,lines 31-55; col. 12, line 58-col. 13, line 4; and col. 14, lines 13-21). That is also why Koyanagi NEVER teaches or suggests that the tacking of the microbumps is capable, by itself, of securing or bonding the substrates together. Koyanagi instead expressly teaches that:

> "It is also **preferable to bond the first semiconductor substrate to the second semiconductor substrate and the second semiconductor substrate to the third semiconductor substrate by injecting a fluid adhesive into the gaps between the semiconductor substrates**, and an **epoxy adhesive is particularly preferable** as the fluid adhesive. The **use of a fluid adhesive for bonding the semiconductor substrates together** make possible uniform injection of an adhesive between the semiconductor substrates. Among fluid adhesives, epoxy fluid adhesives are highly unlikely to generate bubbles, which would adversely affect the electrical performance of the three-dimensional semiconductor integrated circuit apparatus" (col. 4, lines 33-45.) [emphasis added]

At best, it appears that the tacking of the microbumps is an interim step used to keep the substrates in alignment while the *real* bonding (via the injected and hardened epoxy adhesive) is taking place. Further evidence that Koyanagi is not using microbumps for bonding the substrates together also can be found at col. 11, lines 9-21 and (similarly at col. 14, lines 52-63), where Koyanagi states:

> Although in the foregoing embodiment [FIG. 4] the first integrated circuit and the second integrated circuit are **electrically connected via micro-bumps**, and so are the third integrated circuit and the end of the embedded wiring of the second semiconductor substrate, they may as well be **electrically connected** by some other contact members. Though in this embodiment micro-bumps are formed on both surfaces of the semiconductor substrates and the two semiconductor substrates are bonded together [in

> FIG. 4, bonded together using epoxy] so that opposite micro-bumps overlap each other, **electrical connection may be accomplished by micro-bumps on only one side** as illustrated in FIG. 5, so that micro-bumps need to be formed on only one of the substrates. [emphasis added]

As the above passage illustrates, Koyanagi states that, for electrical connection, microbumps need to be formed only one substrate. If tacking of microbumps truly were acting (or capable of acting) to secure or bond together the two substrates , as "secure" and "bond" are understood in the art, such "tacking" would be impossible with microbumps formed on only one of the two substrates. The tacking as Koyanagi describes it requires another microbump to tack to. Consequently, the tacked microbumps of Koyanagi cannot secure or bond together the substrates of Koyanagi, as required by claims 1, 17, and 40. Accordingly, Applicants submit that Koyanagi fails to teach or suggest each and every limitation of claim 1, 17, and 40.

For at least the above reasons, Applicants submit that the rejection of independent claims 1, 17, and 40 under 35 U.S.C. §102(b) is improper and should be removed.

Claims 2, 4-8, 10-13 and 18 - 39 each depend, either directly or indirectly from one of independent claims 1 and 17 and thus include the limitations of either claim 1 or 17, respectively. Accordingly, the rejection of Claims 2, 4-8, 10-13 and 18 - 39 under 35 U.S.C. §102(b) is also improper and should be removed,

The Rejections under 35 U.S.C. §103(a)

The Examiner rejects claims 14-16 under 35 U.S.C. §103(a) as being obvious in view Koyanagi (U.S. Pat. No. 6,525,415) in combination with Nulman (U.S. Pat. No. 5,904,562).

Claims 14-16 each depend either directly or indirectly from base claim 1 and thus include each of the limitations of base claim 1. Accordingly, claims 14-16 each call for a conductive interface, which forms at least part of an electrical communication path and secures together the first and second device layers.

As discussed above, Koyanagi neither describes nor suggests a conductive interface that forms at least part of an electrical communication path and secures together the first and second device layers. Nulman also fails to describe or suggest such an element. Thus, the combination of Koyanagi and Nulman cannot render obvious claims 14 –16 since the combination of the references neither describes nor suggests a conductive interface which forms at least part of an electrical communication path and secures together the first and second device layers as called for in each of claims 14 –16.

Accordingly, in view of the above Remarks, Applicants submit that Claims 1, 2, 4-8, 10-40 and 42 and the entire case are in condition for allowance and should be sent to issue and such action is respectfully requested.

The Examiner is respectfully invited to telephone the undersigning attorney if there are any questions regarding this Response or this application.

Respectfully submitted,

Dated: 11 Apr 2008

DALY, CROWLEY, MOFFORD & DURKEE, LLP

By: /csd/

Christopher S. Daly
Reg. No. 37,303
Attorney for Applicant(s)
354A Turnpike Street - Suite 301A
Canton, MA 02021-2714
Tel.: (781) 401-9988, Ext. 111
Fax: (781) 401-9966
*csd@dc-m.com*

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PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | |
|---|---|---|
| Appl. No. | : 10/655,854 | Confirmation No.: 7254 |
| Applicant | : Rafael Reif et al. | |
| Filed | : September 5, 2003 | |
| T.C./A.U. | : 2826 | |
| EXAMINER | : Leonardo Andujar | |
| Docket No. | : MIT-136AUS | |
| Customer No. | : 22494 | |

**REQUEST FOR EXTENSION OF TIME**

MS Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests that the time to file this Request for Continued Examination be extended for four-months under the provisions of 37 C.F.R. §1.136 or any other applicable provision. It is understood that the filing of this RCE will be treated as a request to withdraw the presently pending appeal.

The Examiner is hereby authorized to charge the fee of $1,640 called for by 37 C.F.R. §1.17 to Deposit Account 50-0845.

In the event any additional fee is required, please charge such amount to the Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

Dated: 11 Apr 2008

DALY, CROWLEY, MOFFORD & DURKEE, LLP

By: /csd/
Christopher S. Daly
Reg. No. 37,303
Attorney for Applicant(s)
354A Turnpike Street, Suite 301A
Canton, MA 02021-2714
Tel.: (781) 401-9988, Ext. 111
Fax: (781) 401-9966
*csd@dc-m.com*

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04/17/2008 16:15 7814019966 DCMD PAGE 01/24

**DALY, CROWLEY, MOFFORD & DURKEE, LLP**

**Telephone: 781-401-9988**
**Facsimile: 781-401-9966**

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Date: April 11, 2008

| | | | |
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| Examiner: | Leonardo Andujar | | |
| Group Art: | 2826 | | |
| Company: | U.S. PTO | | |
| **Facsimile Number:** | **571-273-8300** | | |
| Telephone Number | | | |

DOCKETED

**MESSAGE**

RE: U.S. Patent Application of Rafael Reif et al.
Entitled: Multi-Layer Integrated Semiconductor Structure
Filed on: September 5, 2003
**U.S. Appl. No.: 10/655,854**
Our Ref. No.: MIT-136AUS

**PLEASE CONFIRM RECEIPT OF THIS FACSIMILE TRANSMISSION.**

**THANK YOU.**

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PAGE 1/24 * RCVD AT 4/11/2008 4:56:21 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/3 * DNIS:2738300 * CSID:7814019966 * DURATION (mm-ss):07-46

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/655,854 | 09/05/2003 | Rafael Reif | MIT-136AUS | 7254 |

22494 7590 06/26/2008

DALY, CROWLEY, MOFFORD & DURKEE, LLP
SUITE 301A
354A TURNPIKE STREET
CANTON, MA 02021-2714

| EXAMINER | |
|---|---|
| ANDUJAR, LEONARDO | |
| ART UNIT | PAPER NUMBER |
| 2826 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 06/26/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@dc-m.com
amk@dc-m.com

DOCKETED

| Notice of Abandonment | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/655,854 | REIF ET AL. | |
| | Examiner | Art Unit | |
| | Leonardo Andújar | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *10 May 2007*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____ ), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☒ A proposed reply was received on *01 October 2007*, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.

   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☐ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.

   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.